IN THE CLAIMS:

Following entry of the present amendment, the claims are as follows:

Claim 1 (withdrawn). A strained silicon fin structure comprising

an insulator substrate:

a silicon seed fin structure disposed on the substrate; and

a strained channel layer fabricated on the seed fin structure, the channel layer material having a lattice constant different than that of the seed fin material,

whereby the channel layer strain is the result of the lattice mismatch between the channel layer material and the seed fin material.

Claim 2 (withdrawn). A strained fin structure as in claim 1 further comprising an underseed layer disposed between the seed fin structure and the substrate, the underseed layer material having a lattice constant different than that of the seed fin material, whereby the seed fin structure is under strain due to the lattice mismatch between the underseed layer material and the seed fin material.

Claim 3 (withdrawn). A strained silicon fin structure as in claim 1 further comprising a hard mask layer on the seed fin structure.

Claim 4 (withdrawn). A strained silicon finFET device comprising

an insulator substrate;

A source and a drain sandwiching a strained channel region disposing on the substrate, the strained channel comprising

- a gate dielectric layer disposed on the strained channel; and
- a gate over the strained channel and electrically isolated therefrom by the gate dielectric.

Claim 5 (withdrawn). A strained silicon finFET device as in claim 4 wherein the seed fin structure material is silicon germanium or silicon.

Claim 6 (withdrawn). A strained silicon finFET device as in claim 4 wherein the channel layer material is epitaxial silicon, epitaxial silicon germanium, epitaxial carbon doped silicon, or epitaxial carbon doped silicon germanium.

Claim 7 (withdrawn). A strained silicon finFET device as in claim 4 further comprising a hard mask layer on the seed fin structure.

Claim 8 (withdrawn). A strained silicon finFET device as in claim 4 further comprising an underseed layer disposed between the seed fin structure and the substrate, the underseed layer material having a lattice constant different than that of the seed fin material, whereby the seed fin structure is under strain due to the lattice mismatch between the underseed layer material and the seed fin material.

Claim 9 (withdrawn). A strained silicon finFET device as in claim 4 further comprising doping implantation for the strained channel and the source and drain.

Claim 10 (withdrawn). A strained silicon finFET device as in claim 4 wherein the source region and the drain region include a lightly doped region extending to the channel region.

Claim 11 (withdrawn). A strained silicon finFET device as in claim 4 further comprising silicidation of the gate, source and drain.

Claim 12 (currently amended). A method of fabricating a strained silicon finFET device, comprising the steps of:

a) providing a silicon on insulator substrate having a silicon-containing multilayer on an insulator layer;

b) patterning the multilayer into a source region and a drain region sandwiching a seed channel region, the seed channel being a seed fin structure;

c) depositing an epitaxial channel layer onto the seed fin structure, the channel layer material having a lattice constant ~~different~~ smaller than that of the seed fin material, wherein the epitaxial channel layer becomes a tensile strained channel layer due to the lattice mismatch between the channel layer and the seed fin structure;

d) forming a gate dielectric layer on the epitaxial strained channel; and

e) forming a gate over the epitaxial strained channel.

Claim 13 (original). A method as in claim 12 wherein the silicon on insulator substrate is an SOI substrate wherein the silicon-containing multilayer comprises a silicon layer.

Claim 14 (original). A method as in claim 12 wherein the silicon on insulator substrate is an SGOI substrate wherein the silicon-containing multilayer comprises a silicon germanium layer.

Claim 15 (original). A method as in claim 14 wherein the germanium content of the silicon germanium seed fin is between 10% to 100%.

Claim 16 (original). A method as in claim 12 wherein the epitaxial channel layer is a silicon layer, a silicon germanium layer, a carbon doped silicon layer, or a carbon doped silicon germanium layer.

Claim 17 (original). A method as in claim 12 wherein the patterning of the source, drain and channel regions from the multilayer comprises the steps of:

b1) providing a patterned mask on the multilayer;

b2) patterning the multilayer according to the patterned mask to define source, drain and channel regions; and

b3) removing the patterned mask.

Claim 18 (original). A method as in claim 12 further comprising a step c1 after step c:

c1) doping the channel region.

Claim 19 (original). A method as in claim 12 wherein the formation of the gate comprises the steps of:

e1) depositing a gate material layer;

e2) doping the gate material layer;

e3) providing a patterned mask on the gate material layer;

e4) patterning the gate material layer according to the patterned mask to define the gate; and

e5) removing the patterned mask.

Claim 20 (original). A method as in claim 12 further comprising a step f after step e:

f) forming lightly doped region (LDD) and halo regions between the channel region and the source and drain regions.

Claim 21 (original). A method as in claim 12 further comprising the following steps after step e:

g) forming dielectric spacers between the gate and the source and drain regions.

h) doping the source and drain regions.

i) forming salicide of the gate, source and drain regions.

Claim 22 (original). A method as in claim 12 wherein the multilayer comprises

a first silicon-containing layer; and

a second silicon-containing layer, the second silicon-containing layer material having a lattice constant different than that of the first silicon-containing layer, wherein the second silicon-containing layer becomes a strained layer due to the lattice mismatch between the second silicon-containing layer and the first silicon-containing layer.

Claim 23 (original). A method as in claim 22 wherein the multilayer is formed by

providing a silicon on insulator substrate having a first silicon-containing layer on an insulator; and

depositing a second silicon-containing layer on the silicon on insulator substrate, the second silicon-containing layer material having a lattice constant different than that of the first silicon-containing layer.

Claim 24 (original). A method as in claim 22 wherein the thickness of the first silicon-containing layer is between 5 nm to 20 nm.

Claim 25 (original). A method as in claim 22 wherein the first silicon-containing layer is a silicon layer and the second silicon-containing layer is a silicon germanium layer.

Claim 26 (original). A method as in claim 25 wherein the germanium content of the silicon germanium layer is between 10% to 50%.

Claim 27 (original). A method as in claim 12 wherein the top most layer of the multilayer comprises a hard mask layer.

Claim 28 (original). A method as in claim 12 wherein the height of the seed fin structure is between 10 nm to 200 nm.

Claim 29 (original). A method as in claim 12 wherein the width of the seed fin structure is between 5 nm to 100 nm.

Claim 30 (original). A method as in claim 12 wherein the thickness of the strained channel layer is between 5 nm to 15 nm.

Claim 31 (new). A method of fabricating a strained silicon finFET device, comprising the steps of:

a) providing a silicon on insulator substrate; the silicon on insulator substrate comprising a relaxed silicon germanium layer on an insulator layer;

b) patterning the relaxed silicon germanium layer into a source region and a drain region sandwiching a seed channel region, the seed channel being a seed fin structure;

c) depositing an epitaxial silicon channel layer onto the seed fin structure, wherein the epitaxial silicon channel layer becomes a tensile strained silicon channel layer due to the lattice mismatch between silicon and silicon germanium;

d) forming a gate dielectric layer on the epitaxial strained silicon channel; and

e) forming a gate over the epitaxial strained silicon channel.

Claim 32 (new). A method as in claim 31 wherein the deposited epitaxial silicon channel layer comprises germanium component to form a tensile strained silicon germanium channel layer on the seed fin structure, the germanium composition of the channel layer being less than that of the relaxed silicon germanium layer.

Claim 33 (new). A method as in claim 31 further comprising a step a2 after step a:

a2) depositing a hardmask layer onto the relaxed silicon germanium layer;

wherein the deposited hardmask layer is also patterned together with the silicon germanium layer in step b.

Claim 34 (new). A method of fabricating a strained silicon finFET device, comprising the steps of:

a) providing a silicon on insulator substrate; the silicon on insulator substrate comprising a silicon layer on an insulator layer;

a1) depositing a silicon germanium layer onto the silicon layer;

b) patterning the multilayer of silicon germanium layer and silicon layer into a source region and a drain region sandwiching a seed channel region, the seed channel being a seed fin structure;

c) depositing an epitaxial silicon channel layer onto the seed fin structure, wherein the epitaxial silicon channel layer becomes a tensile strained silicon channel layer due to the lattice mismatch between silicon and silicon germanium;

d) forming a gate dielectric layer on the epitaxial strained silicon channel; and

e) forming a gate over the epitaxial strained silicon channel.

Claim 35 (new). A method as in claim 34 wherein the silicon layer of the silicon on insulator substrate comprises germanium component to form a silicon germanium layer on the silicon on insulator substrate, the germanium composition of the silicon germanium of the silicon on insulator substrate being less than that of the subsequently deposited silicon germanium layer.

Claim 36 (new). A method as in claim 34 wherein the deposited epitaxial silicon channel layer comprises germanium component to form a tensile strained silicon germanium channel layer on the seed fin structure, the germanium composition of the channel layer being less than that of the silicon germanium underlayer.

Claim 37 (new). A method as in claim 34 further comprising a step a2 after step a1:

a2) depositing a hardmask layer onto the silicon germanium layer; wherein the deposited hardmask layer is also patterned together with the multilayer of strained silicon germanium layer and silicon layer in step b.

Claim 38 (new). A method of fabricating a strained silicon finFET device, comprising the steps of:

a) providing a silicon on insulator substrate; the silicon on insulator substrate comprising a relaxed silicon germanium layer on an insulator layer;

a1) depositing an epitaxial silicon channel layer onto the relaxed silicon germanium layer wherein the epitaxial silicon channel layer becomes a tensile strained silicon channel layer due to the lattice mismatch between silicon and silicon germanium;

b) patterning the multilayer of epitaxial silicon channel layer and silicon germanium layer into a source region and a drain region of a fin structure;

d) forming a gate dielectric layer on the epitaxial strained silicon channel; and

e) forming a gate over the epitaxial strained silicon channel.

Claim 39 (new). A method as in claim 38 wherein the silicon layer of the silicon on insulator substrate comprises germanium component to form a silicon germanium layer on the silicon on insulator substrate, the germanium composition of the silicon germanium of the silicon on insulator substrate being less than that of the subsequently deposited silicon germanium layer.

Claim 40 (new). A method as in claim 38 further comprising a step a2 after step a1:

a2) depositing a hardmask layer onto the epitaxial silicon channel layer;

wherein the deposited hardmask layer is also patterned together with the multilayer of epitaxial silicon channel layer and silicon germanium layer in step b.

Claim 41 (new). A method of fabricating a strained silicon finFET device, comprising the steps of:

a) providing a silicon on insulator substrate; the silicon on insulator substrate comprising a silicon layer on an insulator layer;

b) patterning the silicon layer into a source region and a drain region sandwiching a seed channel region, the seed channel being a seed fin structure;

c) depositing an epitaxial carbon doped silicon channel layer onto the seed fin structure, wherein the epitaxial silicon carbon channel layer becomes a tensile strained silicon channel layer due to the lattice mismatch between silicon carbon and silicon;

d) forming a gate dielectric layer on the epitaxial strained silicon channel; and

e) forming a gate over the epitaxial strained silicon channel.